

PRIOR ART

FIG. 1

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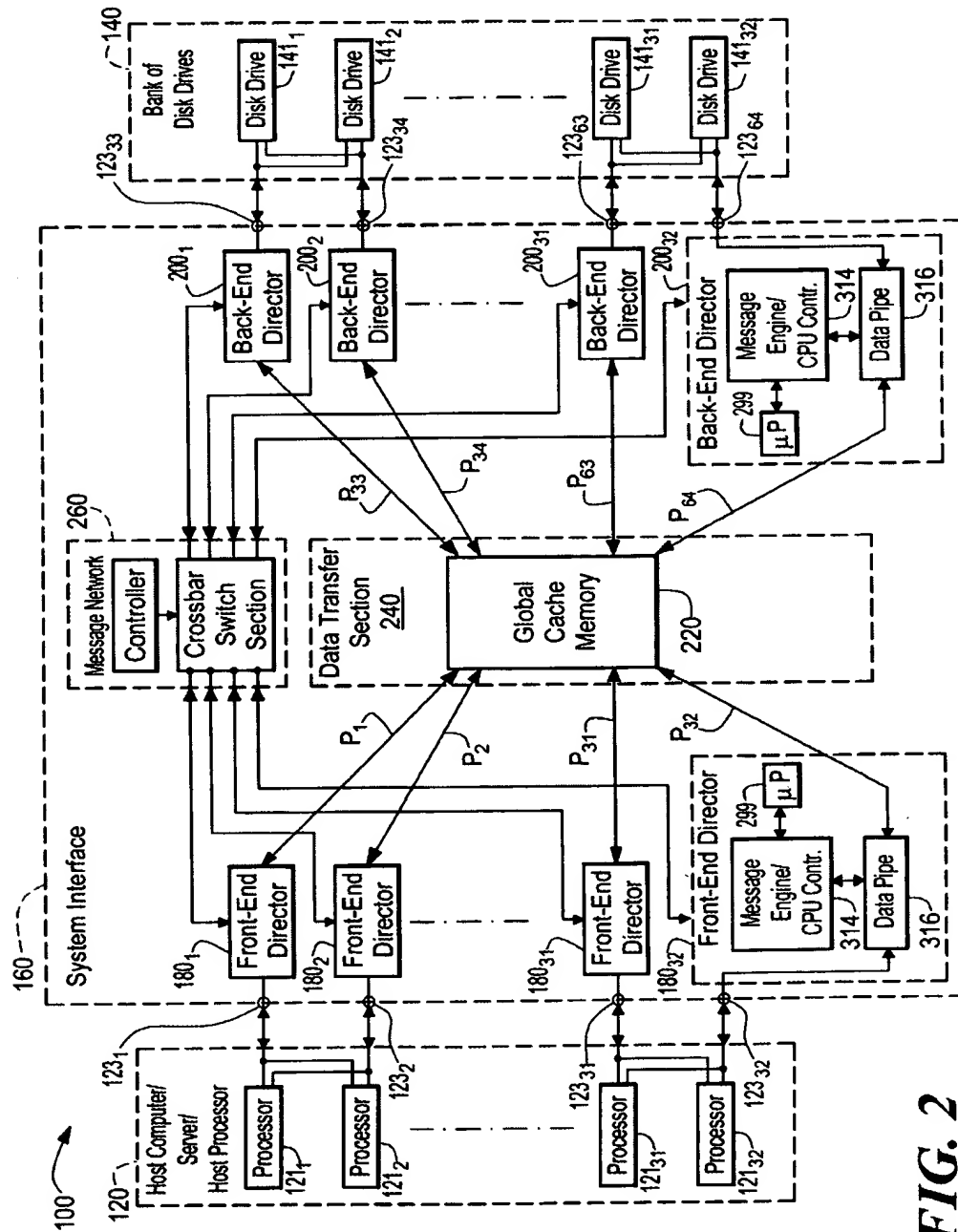
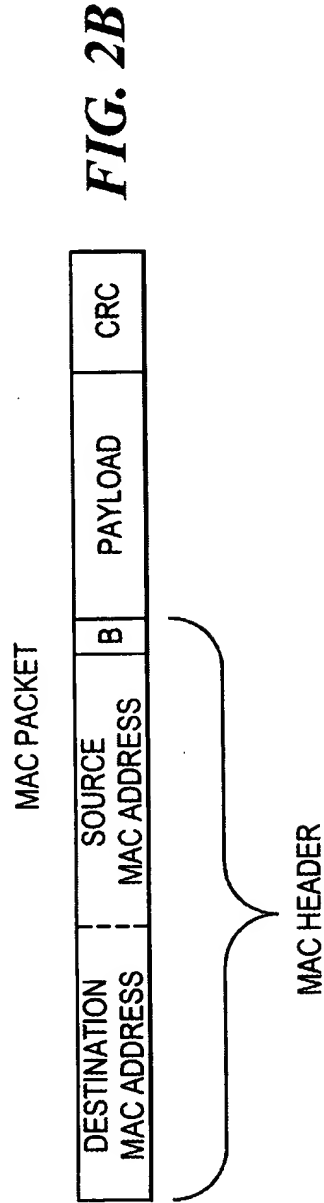
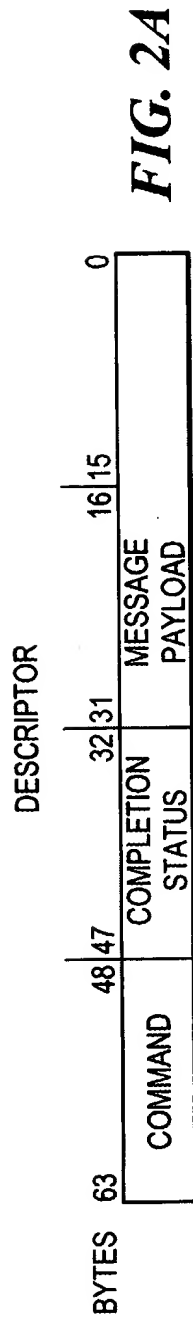


FIG. 2

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FIG. 3

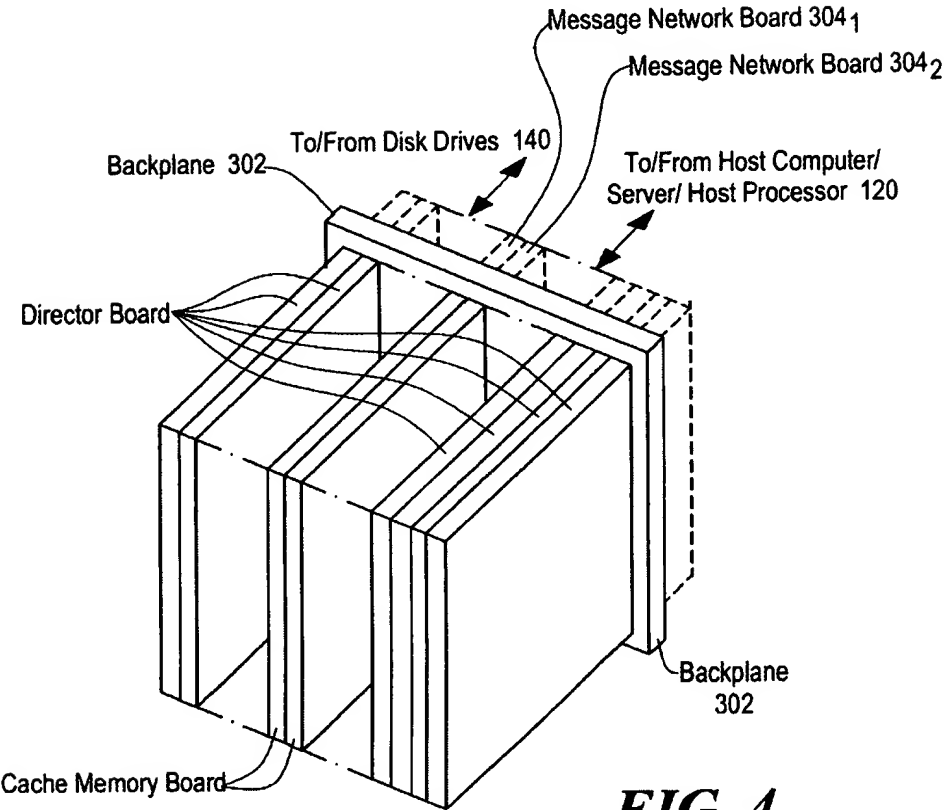
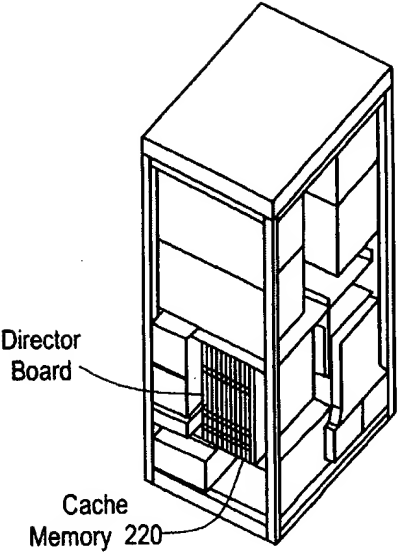
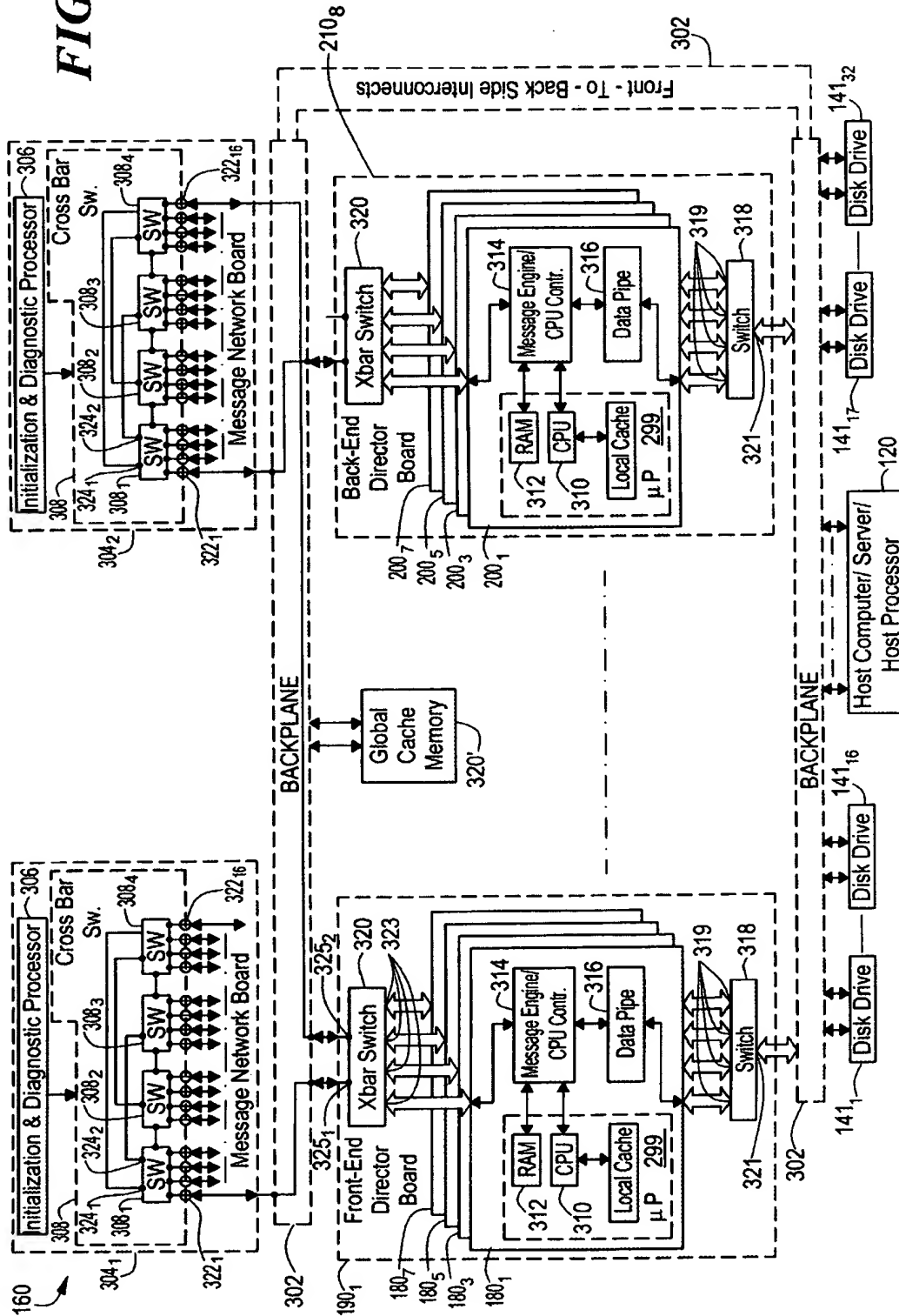


FIG. 4

FIG. 5



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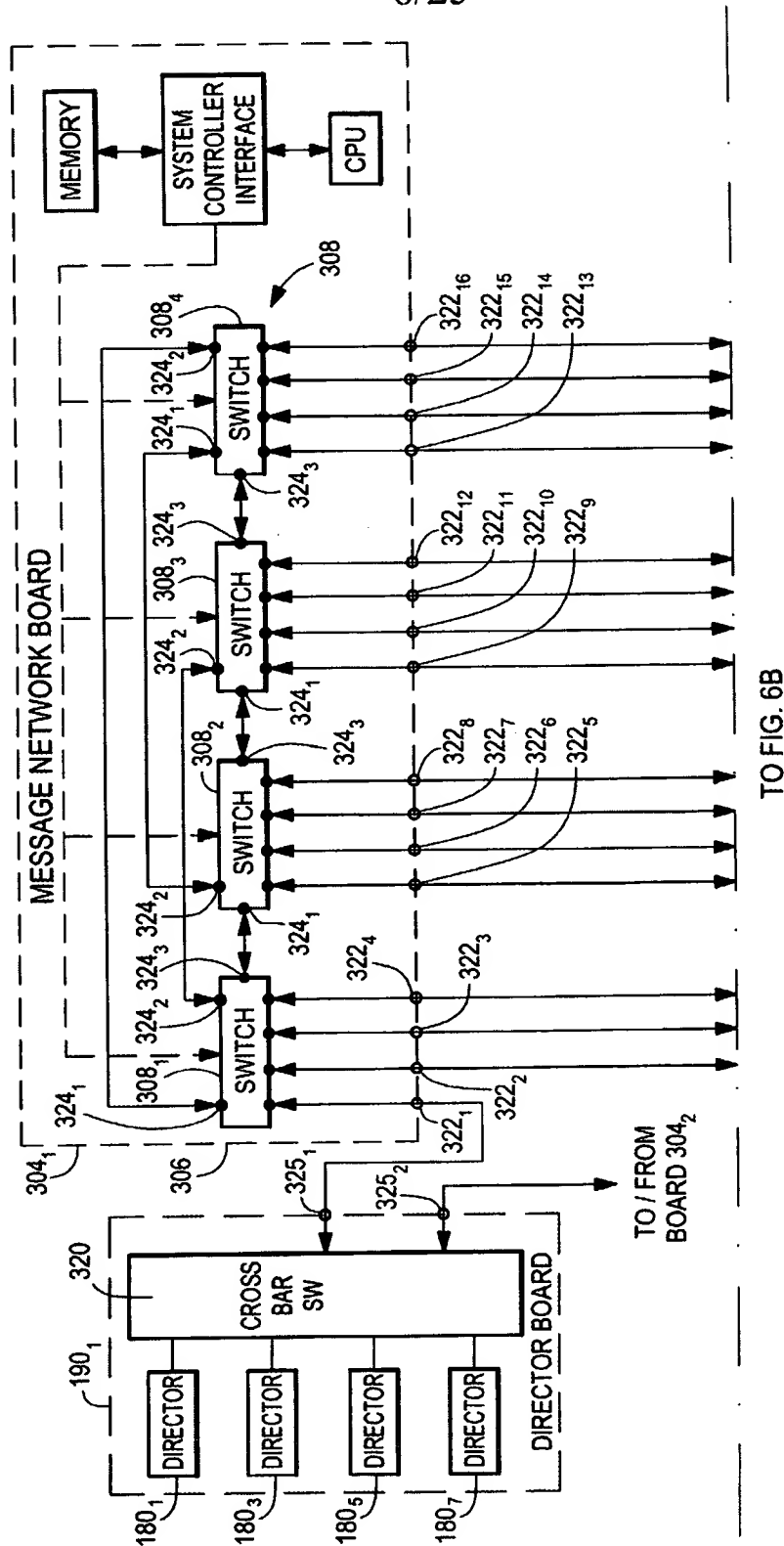
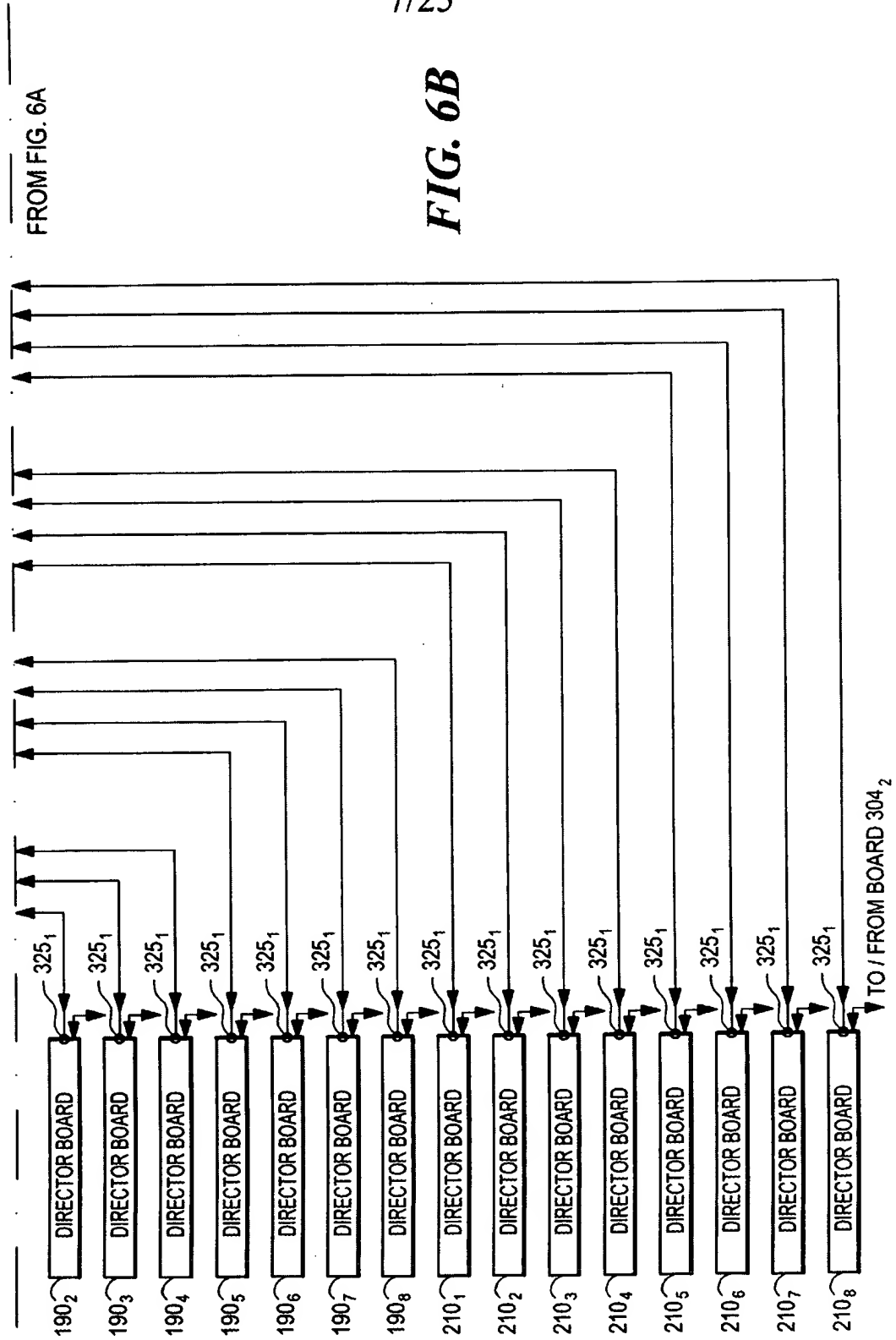


FIG. 6A

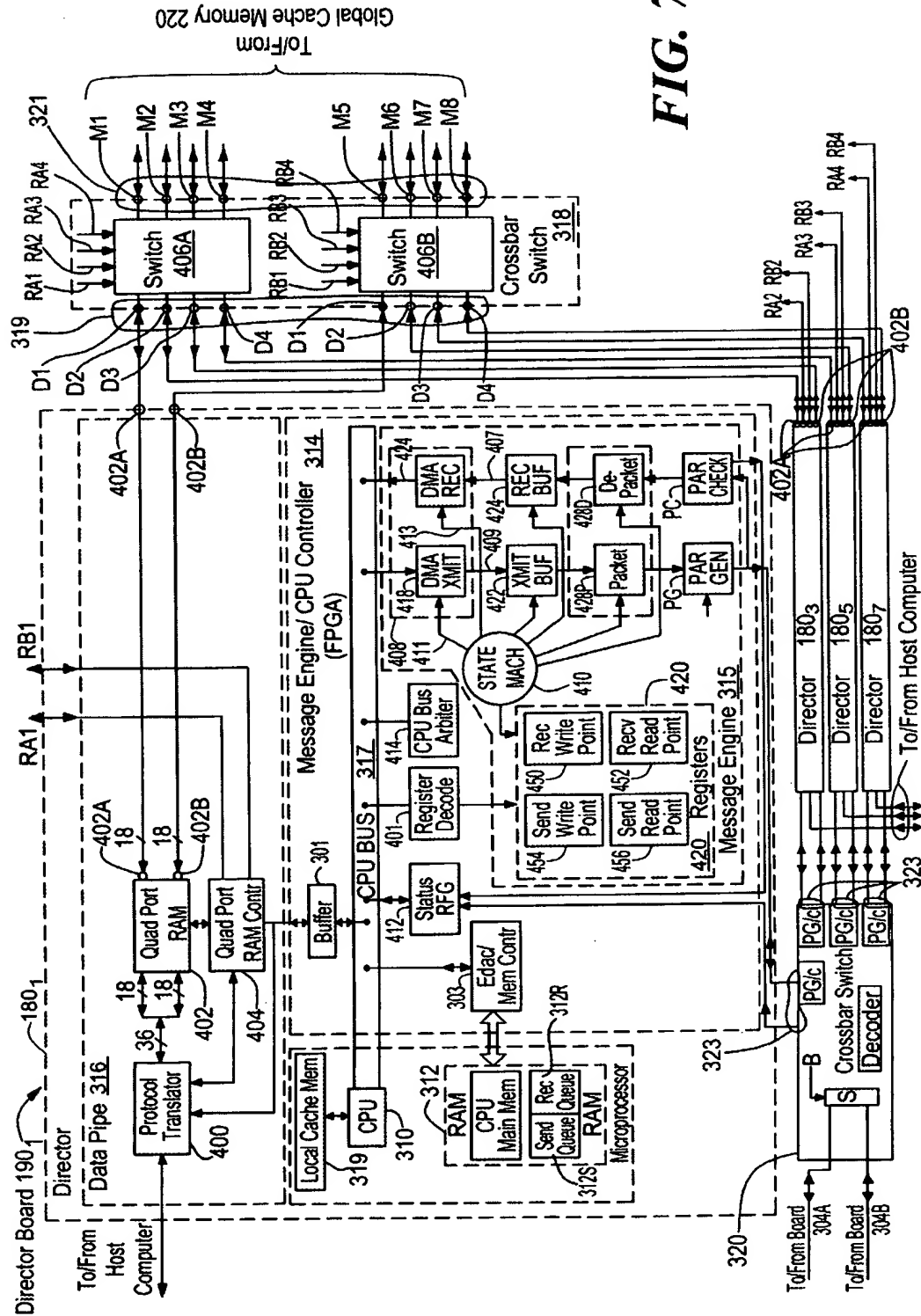
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FIG. 6B



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FIG. 7



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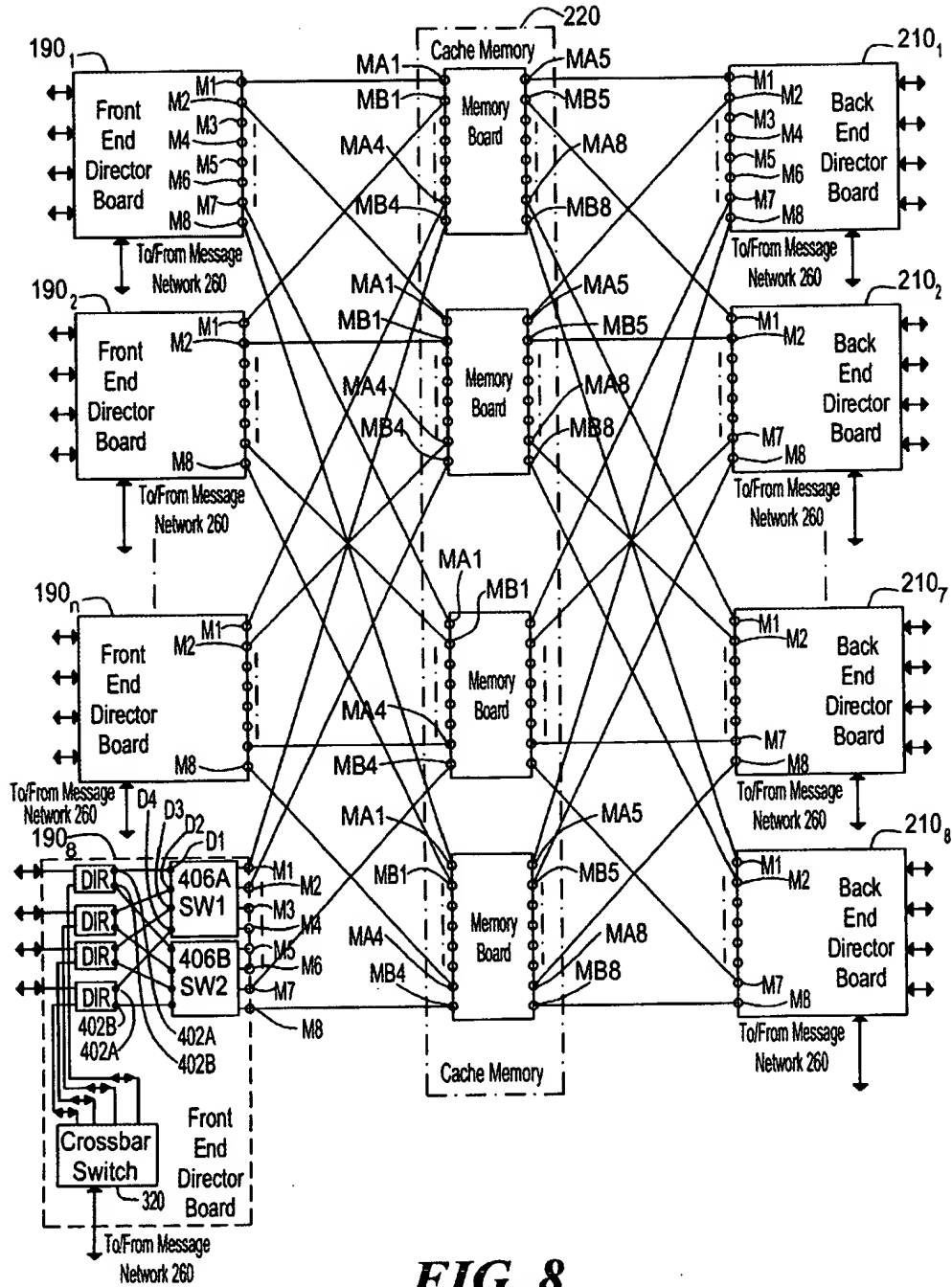


FIG. 8

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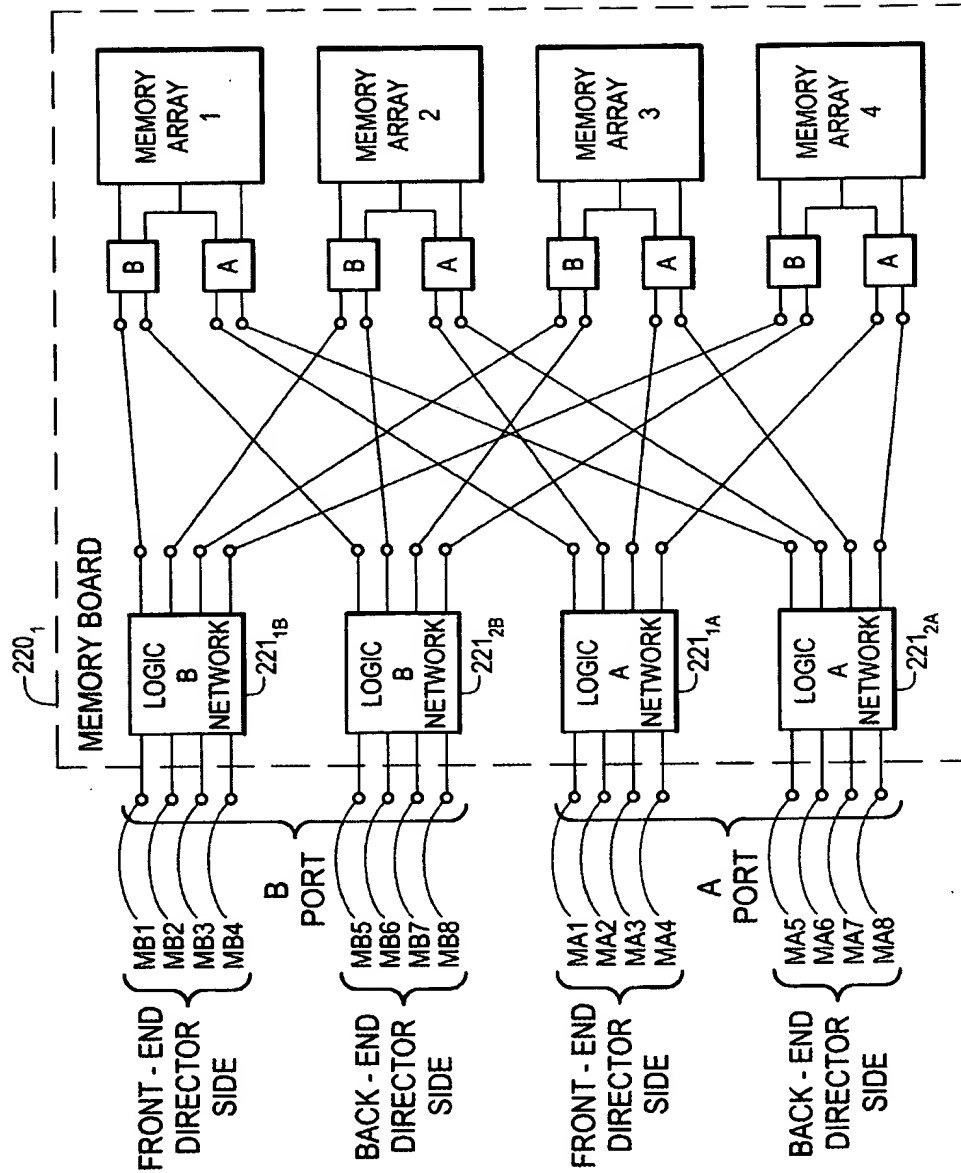


FIG. 8A

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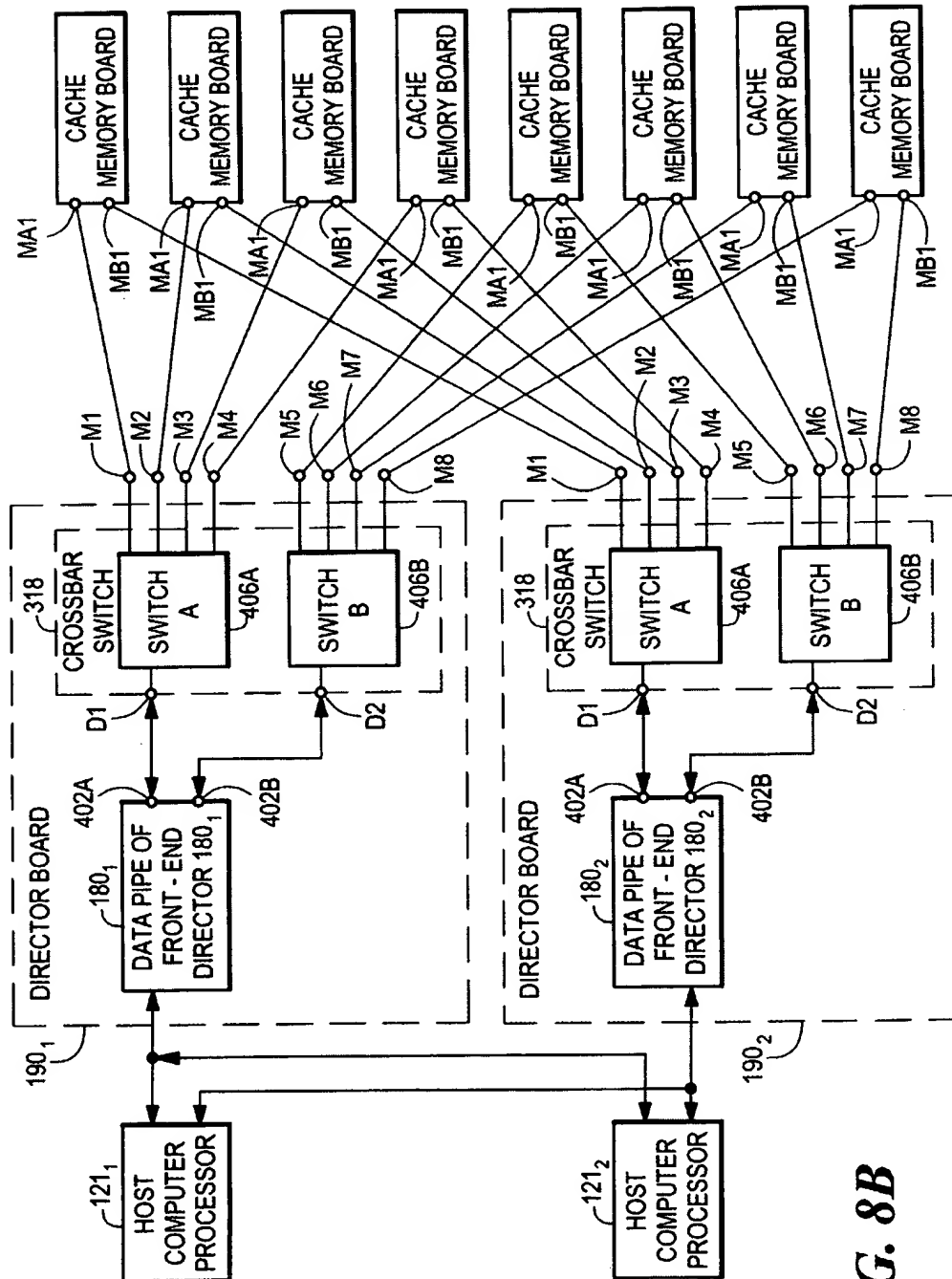


FIG. 8B

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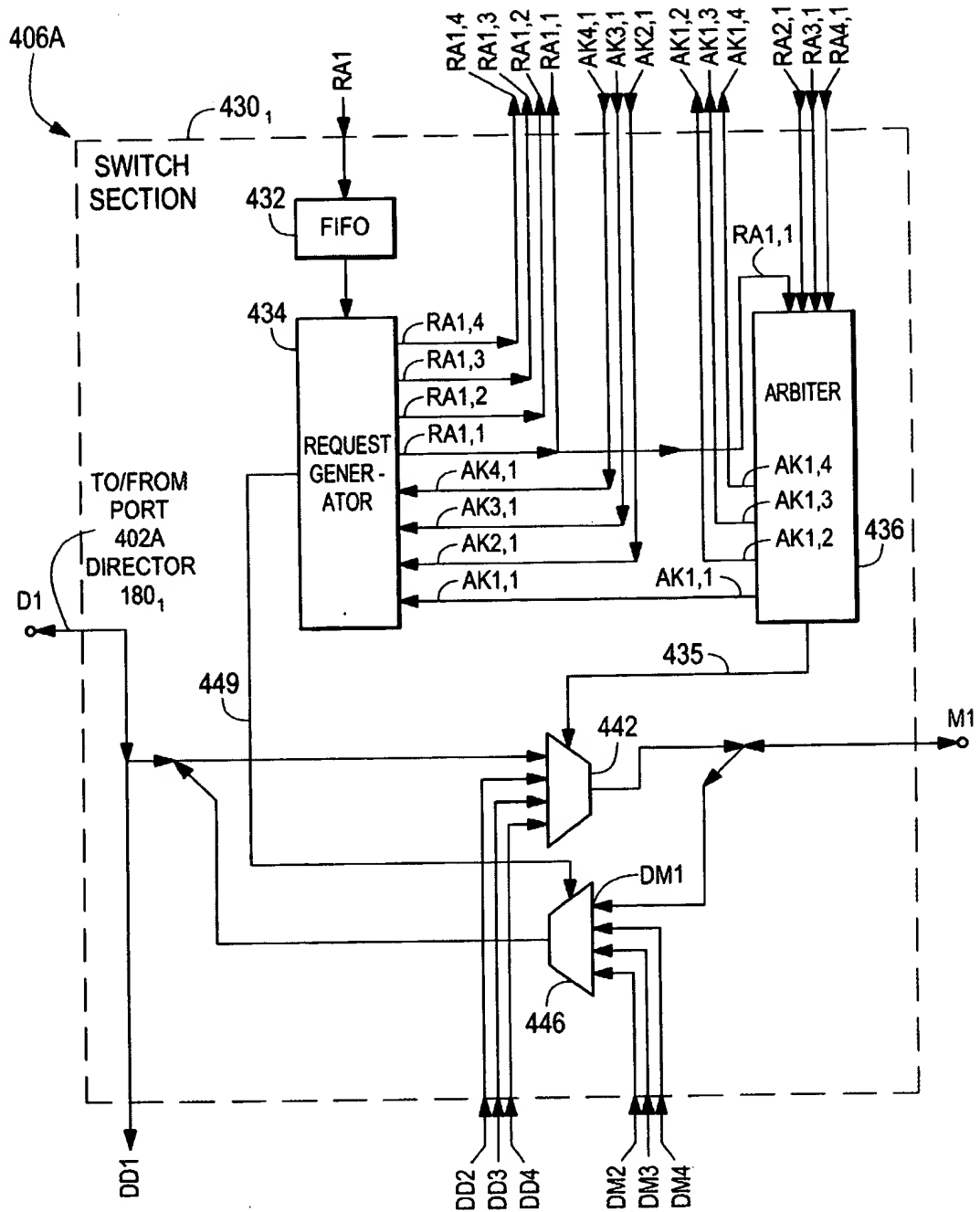


FIG. 8C

FIG. 8C-1
FIG. 8C-2

FIG. 8C-1

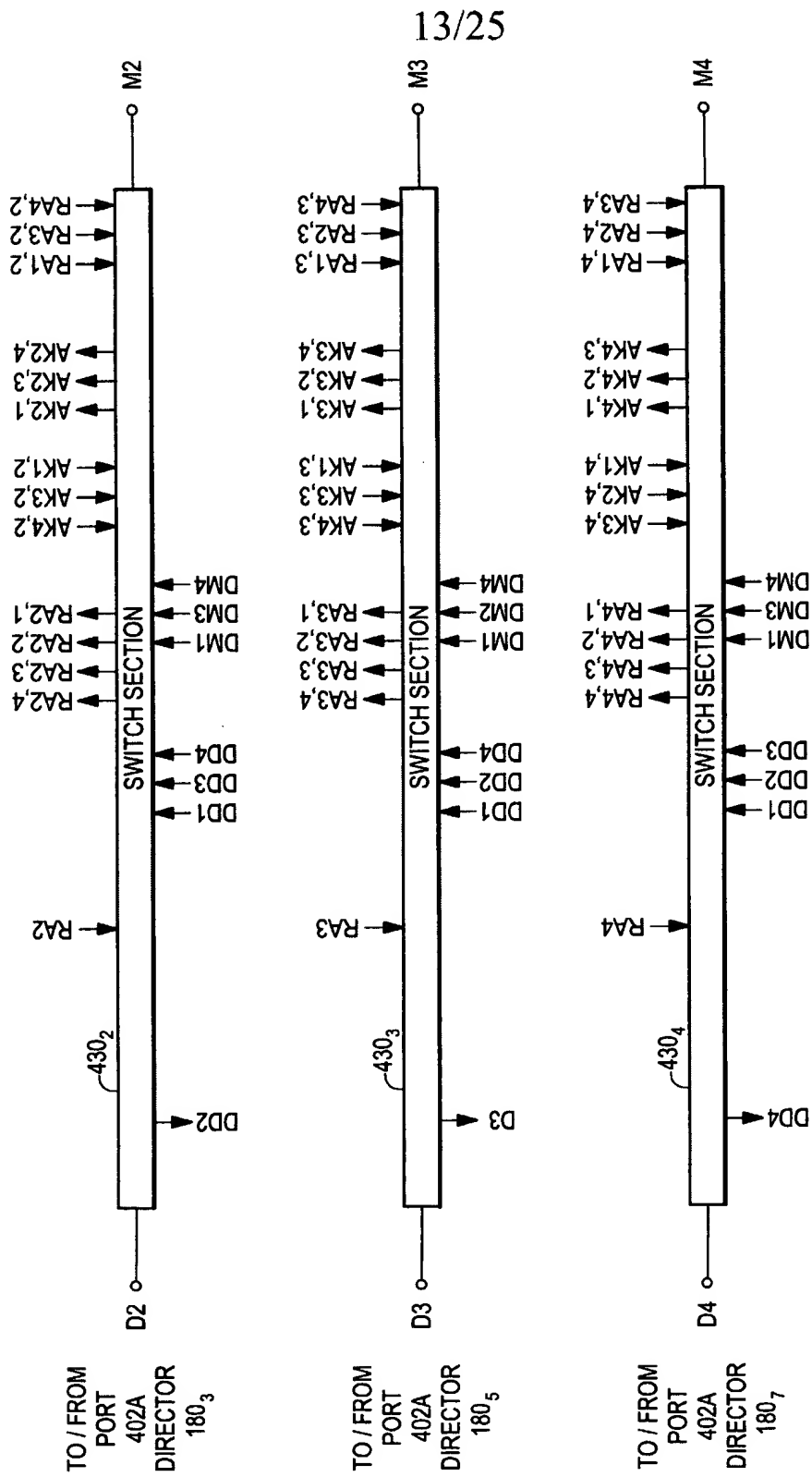


FIG. 8C-2

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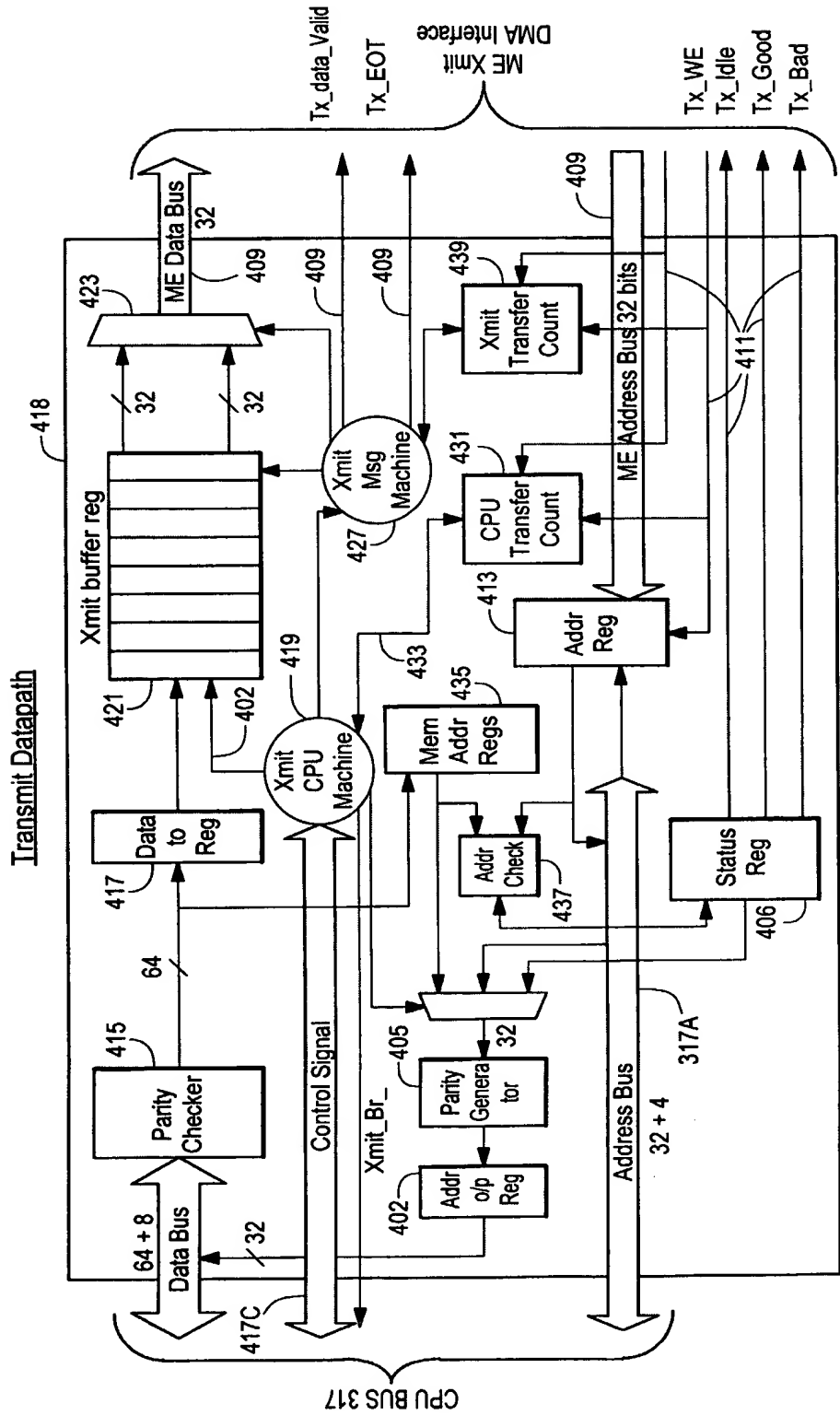


FIG. 9

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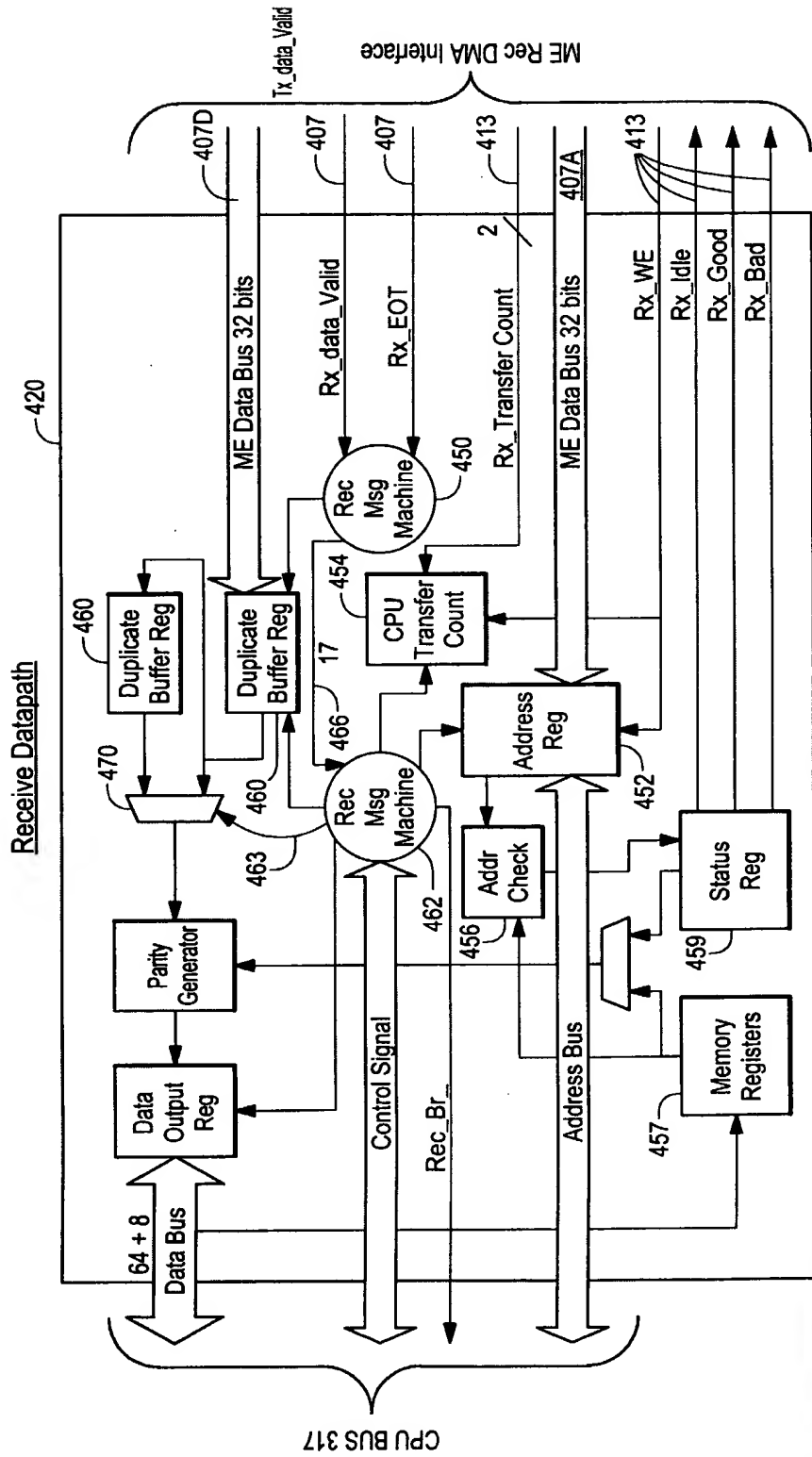


FIG. 10

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FIG. 11

FIG. 11A

FIG. 11B

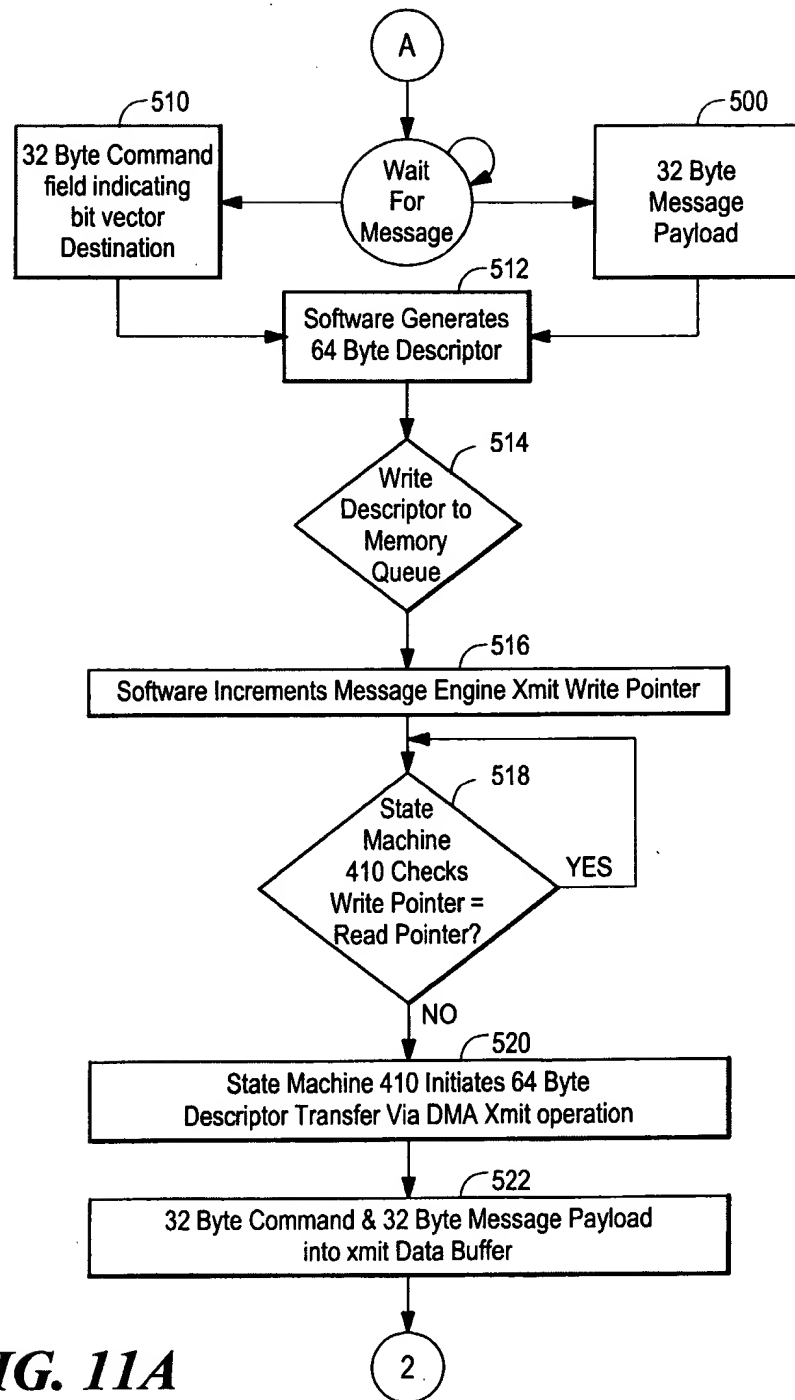


FIG. 11A

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Message Bus Send Operation Continued

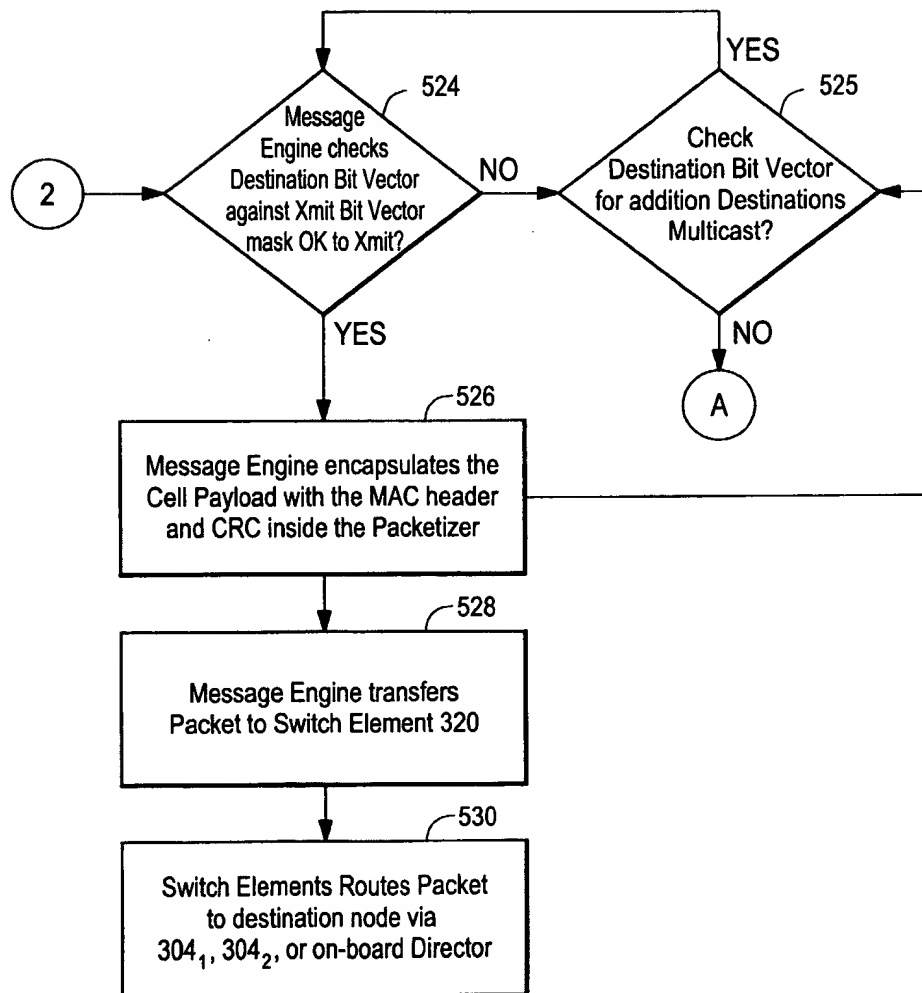
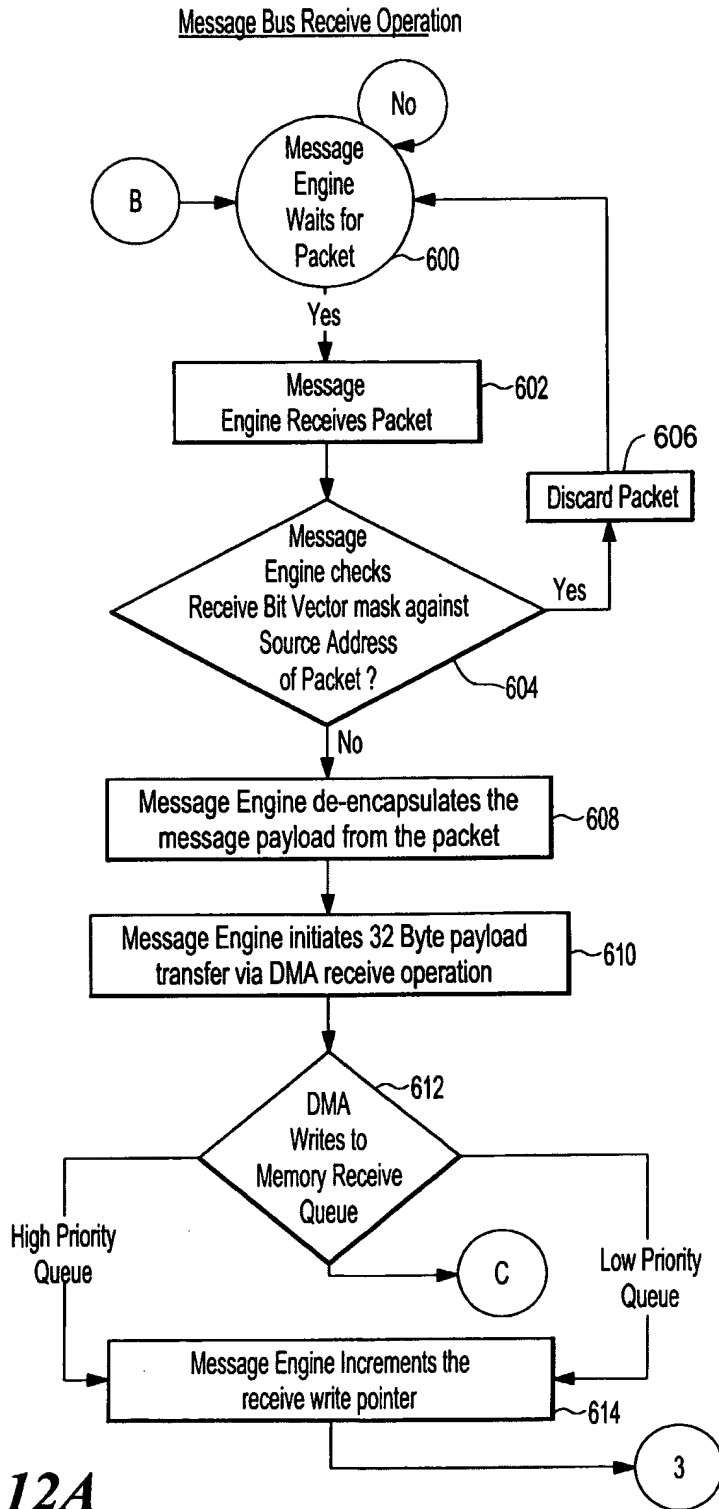
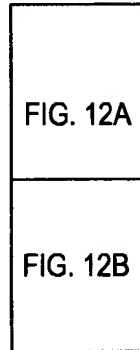


FIG. 11B



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FIG. 12



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Message Bus Receive Operation Continued

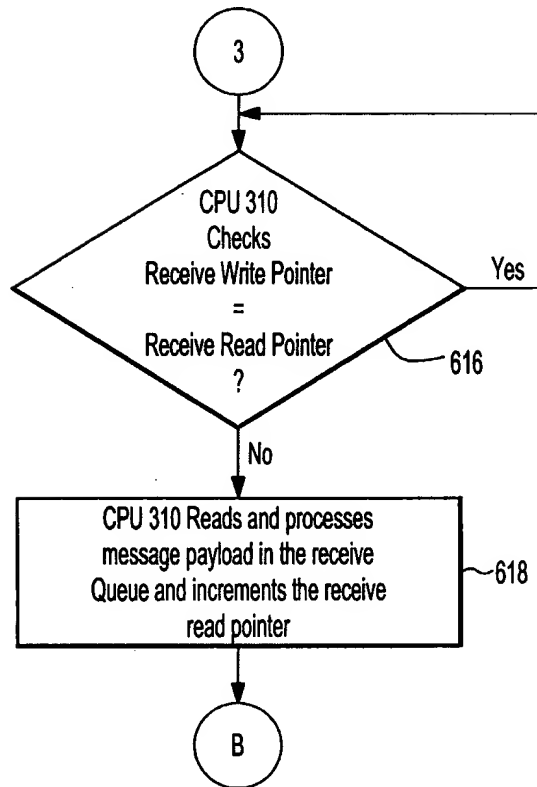


FIG. 12B

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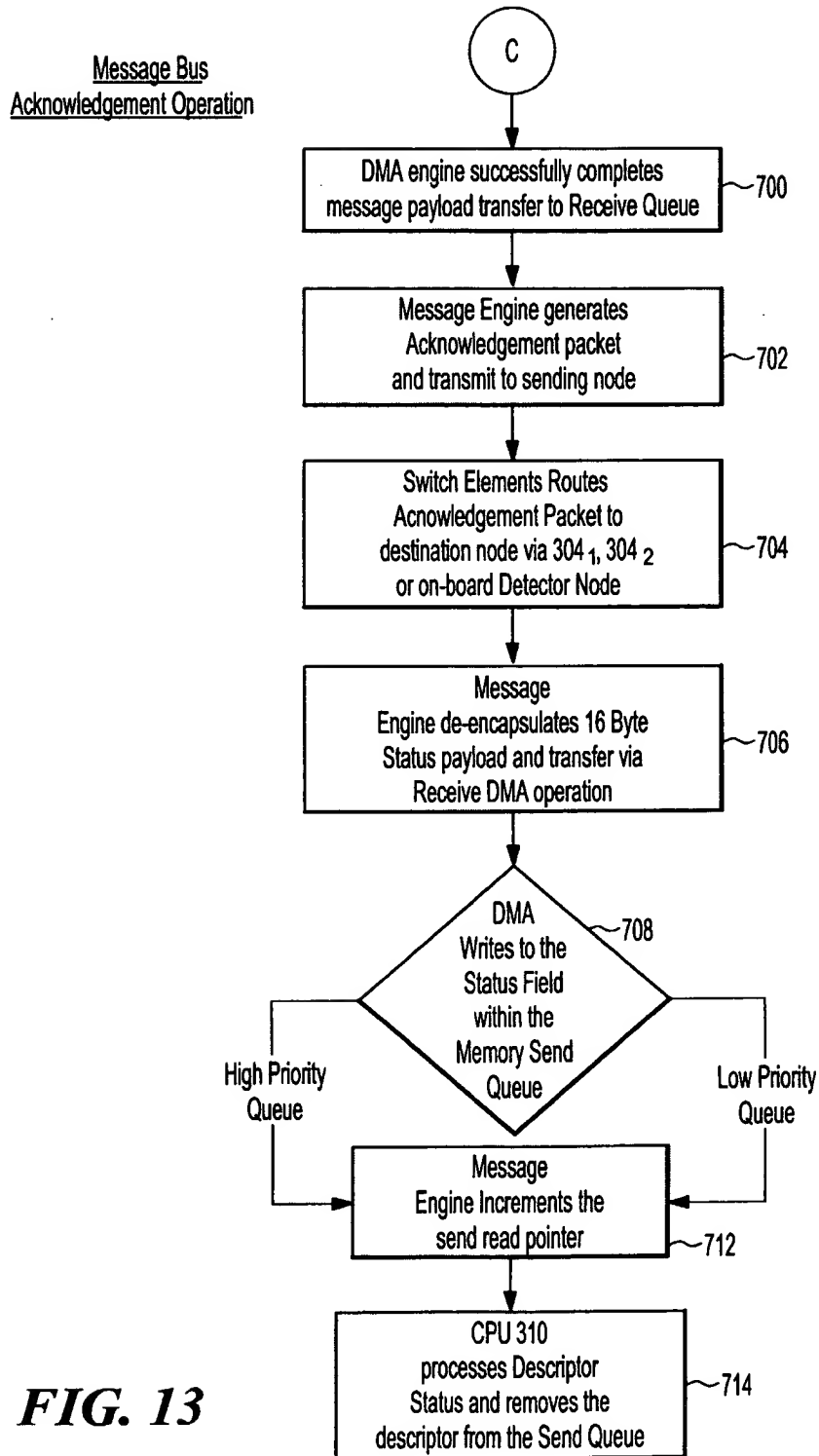


FIG. 13

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Xmit CPU flow

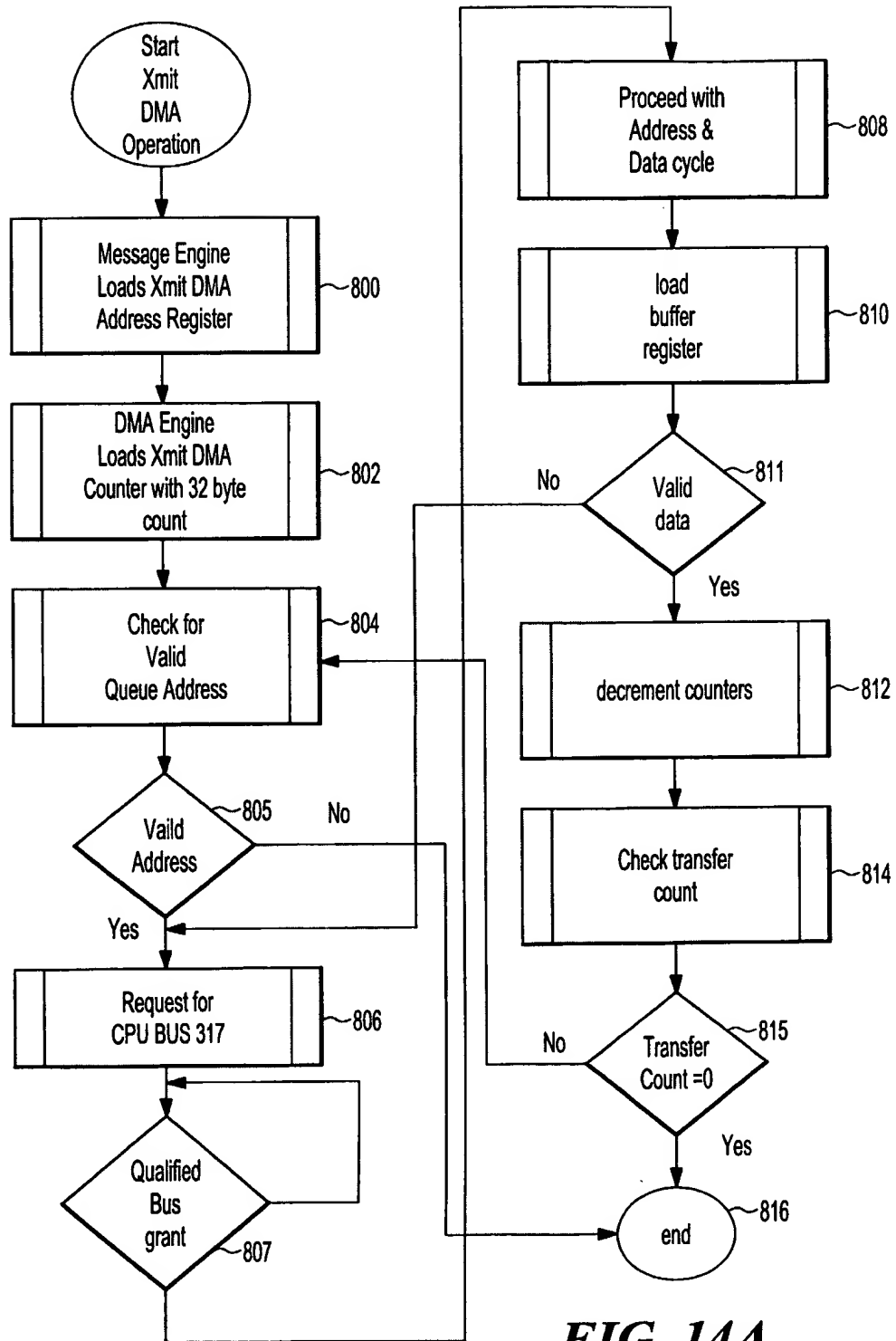


FIG. 14A

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Xmit Msg flow

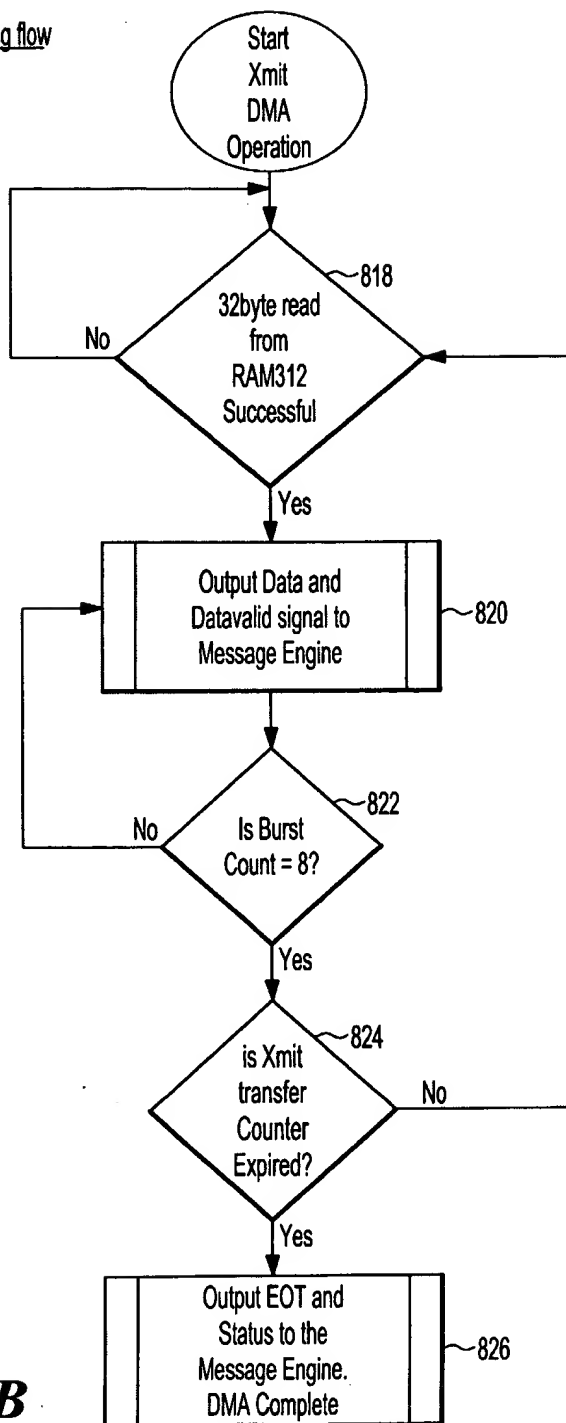


FIG. 14B

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Rec msg flow

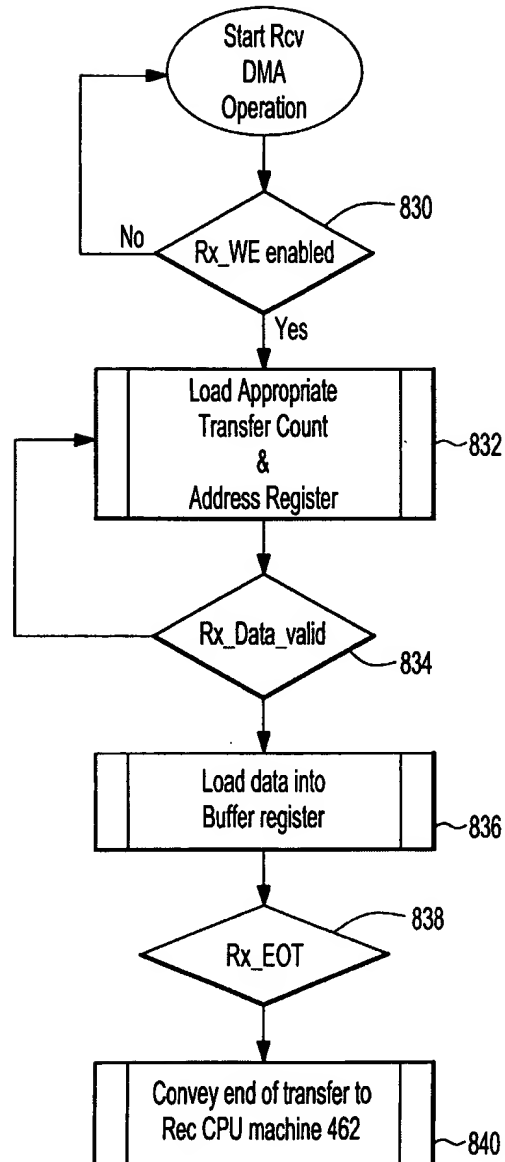


FIG. 15A

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Rec cpu flow

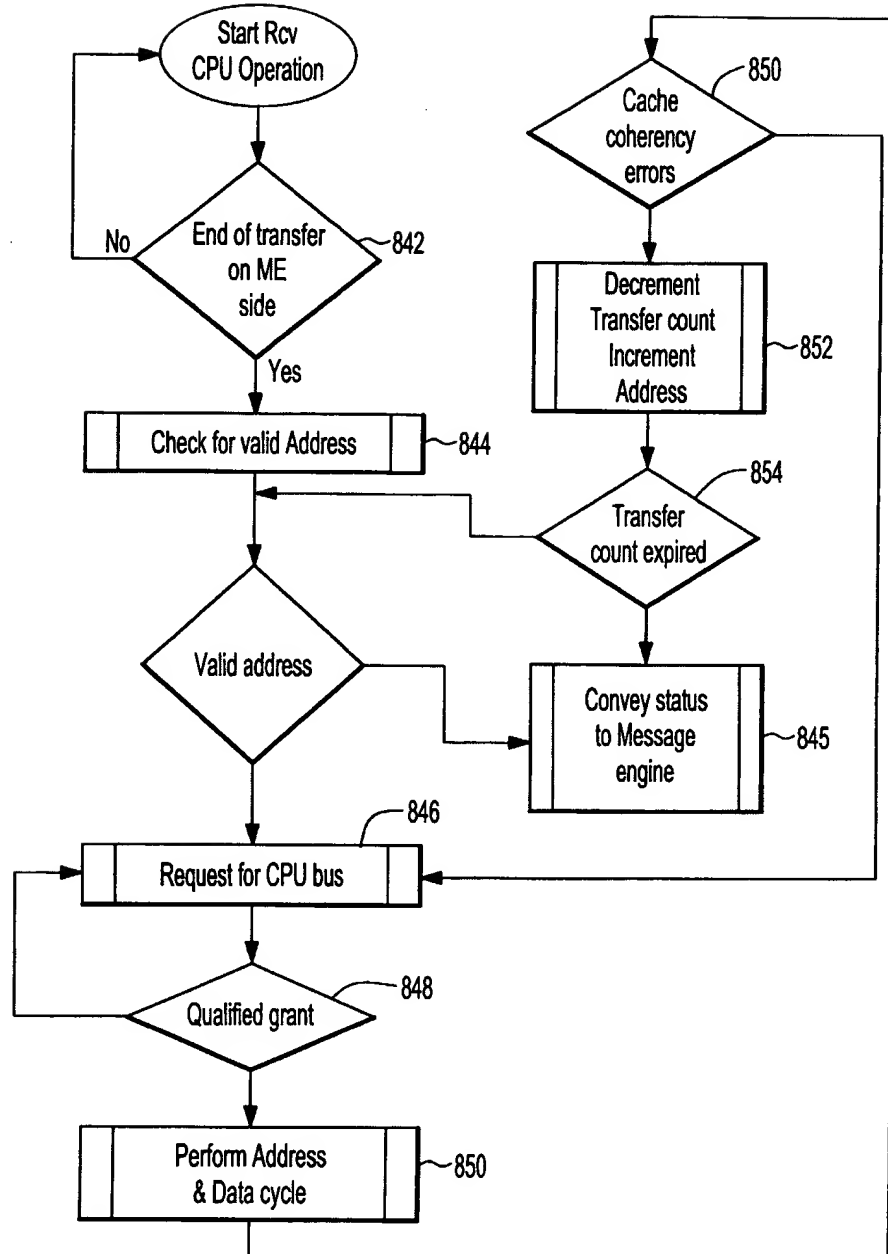


FIG. 15B